Semiconductor Integrated Circuit Processing Technology

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In particular, progress in miniaturization of semiconductor integrated circuit processing technology, scaled by when the threshold voltage of the power supply voltage and transistor has been low voltage, normal operation time of high-speed processing and for both low leakage current in the standby it relates to technology.

Front-end technology features include shallow trench isolation, retrograde wells, shallow abrupt source/drain extensions, halo implants, deep source/drain, and cobalt salicidation. Figure 7 shows a front-end cross section of the technology. This process technology uses dual damascene copper to reduce the resistances of the interconnects. Fluorinated SiO2 (FSG) is used as an inter-level dielectric (ILD) to reduce the dielectric constant; the dielectric constant $k$ is measured to be 3.6. Figure 17 is a cross-section Scanning Electron Micrograph (SEM) image showing the dual damascene interconnects.